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INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 6 : H04N 3/14

A1

(11) International Publication Number: **WO 99/48281**

(43) International Publication Date: 23 September 1999 (23.09.99)

(21) International Application Number: PCT/US99/05830

(22) International Filing Date: 16 March 1999 (16.03.99)

(30) Priority Data:
60/078,172 16 March 1998 (16.03.98) US

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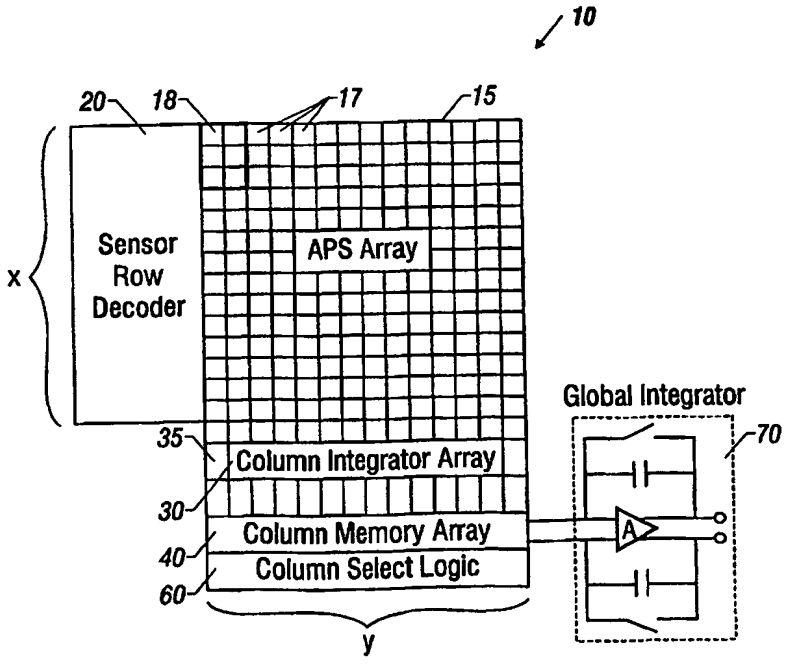
(81) Designated States: AE, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CU, CZ, DE, DK, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, UA, UG, UZ, VN, YU, ZA, ZW, ARIPO patent (GH, GM, KE, LS, MW, SD, SL, SZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).

Published
With international search report.
Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.

(54) Title: CMOS INTEGRATION SENSOR WITH FULLY DIFFERENTIAL COLUMN READOUT CIRCUIT FOR LIGHT ADAPTIVE IMAGING

(57) Abstract

An imager (10) that is better suited for low–light detection capability. In accordance with a preferred embodiment, the imager may be easily configured to provide an imager (10) having multi–resolution capability where SNR can be adjusted for optimum low–level detectibility. Multi–resolution signal processing functionality is provided on–chip to achieve high speed imaging, employs an improved pixel binning approach with fully differential circuits situated so that all extraneous and pick–up noise is eliminated. The current implementation requires no frame transfer memory, thereby reducing chip size. The reduction in area enables larger area format light adaptive imager implementations.



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CMOS INTEGRATION SENSOR WITH FULLY DIFFERENTIAL COLUMN READOUT CIRCUIT FOR LIGHT ADAPTIVE IMAGING

Statement as to Federally Sponsored Research

The invention described herein was made in the performance of work under a NASA contract, and is subject to the provisions of Public Law 96-517 (35 USC 202) in which the Contractor has elected to retain title.

Field of the Invention

The present disclosure is directed to active pixel sensors, and more particularly to multi-resolution active pixel sensor array imagers for light adaptive imaging applications.

Background

The CMOS active pixel sensor ("APS") has permitted the realization of high performance products. Each pixel has an active amplifier that buffers the photosignal. A column-parallel bus readout architecture is often used. In this architecture, the columns are connected to individual signal processing modules, which include, for example, A to D converters, and double sampling elements.

A constant challenge in smart imager technology continues to be how to enhance signal to noise ratio ("SNR") under low illumination conditions.

One way to do this is to trade spatial resolution for SNR by summing neighborhood pixels (pixel binning). A CMOS imager that averages signals from a neighborhood of pixels has been demonstrated in "Programmable Multiresolution CMOS Active Pixel Sensor", in Solid-state

Sensor Arrays & CCD Camera, Proc. SPIE vol. 2654, pp. 72-81, 1996, by Panicacci, et al.

A CMOS imager with frame memory and pixel binning has been demonstrated in a reference titled, "Frame-transfer CMOS Active Pixel Sensor with Pixel Binning', special issue on Solid-State Image Sensors, IEEE Trans. On Electron Devices, vol. 44 (10), pp. 1759-1763, 1997, authored by Pain, Zhou and Fossum.

Summary

The present disclosure is directed to an improved pixel-binning imager. In accordance with a preferred embodiment, the imager may be easily configured to provide an imager having multi-resolution capability where SNR can be adjusted for optimum low-level detectibility.

Further in accordance with the preferred implementation, multi-resolution signal processing functionality is provided on-chip to achieve high speed imaging, as well as low power consumption.

An imager architecture described preferably has an improved pixel binning approach with fully differential circuits situated so that all extraneous and pick-up noise is eliminated. Unlike the frame-transfer APS with pixel binning, the current implementation minimizes the necessary memory, thereby reducing chip size. The reduction in area enables larger area format light adaptive imager implementations.

Brief Description of the Drawings

Fig. 1 is a block diagram of an APS imager with on-chip variable resolution in accordance with the present invention.

Fig. 2 is a more detailed schematic diagram of the APS imager shown in Fig.1.

FIG. 3 shows an exemplary timing diagram for generating two adjacent 3x2 kernels using the imager of the present invention.

Fig. 4 graphically shows expected results of signal detectibility as a function of kernel size achievable by the imager of the present invention,

Description of the Preferred Embodiments

Fig. 1 is a block diagram of an APS imager 10 provided with on-chip variable resolution. Imager 10 is a variable resolution CMOS active pixel imager that enhances SNR at low illumination level. In the preferred embodiment, imager 10 is an x-row by y-column photosensitive array 15 of pixels 17. The imager includes a controller that is programmable to read out any sized kernel 18, where a kernel is an n-row by m-column block of pixels. Each kernel 18 represents the summed value of all the pixel values in its region. In the illustrative example, the kernel 18 is a 3-row by 2-column sized region in array 15.

Imager 10 has a sensor row decoder 20 at the side of array 15. An entire row of pixels is selected for readout at each time. Each pixel 17 is preferably a photogate-type active pixel as shown in Fig. 2, with an in-chip buffer circuit MP2 that is controlled by a photogate transfer signal (TX) enabling readout of integrated charge by lowering the charge barrier. A reset signal (RSTP) and select signal (row) enable the buffered pixel signal to drive the associated column output line, all in a conventional manner.

A column integration array 30 is connected in parallel to the row outputs. An individual column integrator 35 is located at the bottom of the array, associated with each column. Each integrator 35 is associated with a row of pixels. These collectively feed associated column memory 40, which is constituted by y-columns of associated column memory circuits 45, e.g. capacitors. Figure 2 shows details of the single column integrator 35 being coupled to its associated column memory capacitor circuit 45. The signal output from the pixel 17, is connected to the column integrator portion 35 in a differential manner. Two totally different paths to the differential opamp A are shown. One path is through the signal transistor MS, controlled by the control signal PHIS. This leads the signal through capacitor CMS, where it is again controlled through second transistor MMS. A totally parallel path for the reset signal goes through transistor MR, CMR, and MMR. To enable correlated double sampling, a crowbar circuit CB is also provided. The opamp A is connected as a fully differential switched capacitors integrators. Column memory capacitor circuit 45 uses capacitors CLS and CLR and switches MC9 and MC10 for signal and reset levels, respectively. It should be appreciated that an imager 10 with for example 512 more columns of pixels than another imager will possess 512 more column integrators and column memory capacitor circuit pairs 50. Each pair 50 serves a particular column.

In the exemplary embodiment to be described in greater detail below, imager 10 is read out one row at a time. Therefore, at a given time, one row of pixels is sampled simultaneously at the bottom of the column, using appropriate column decoder select logic 60 shown in block

diagrammatic form in Fig. 1. Each pixel 16 across a sampled row is first sampled on the capacitors CMR and CMS inside associated column integrator 35 connected to a particular column. The signal PHIS is pulsed to bring the signal level onto the capacitor CMS, and the signal PHIR is momentarily pulsed to bring the reset level onto the capacitor CMR. These levels are then coupled to the opamp A by pulsing the RDC signals. The opamp differentially integrates using the integrating capacitors CIS and CIR. Double-sampling is carried out using the crowbar switch CB as described later herein. This process continues until all of the rows in a given kernel are summed.

The size of the column integrator scales linearly with the number of columns. For instance, assuming a 1024x1024 imager with a 10 μm pixel, there are 1024 column-integrators 35 and the width of each column-integrator is 10 μm. The total width of column integrator assembly 30 is then 10x1024 μm = 10 cm. The length (height) of CIA 30 is of course fixed at around 2 mm.

As explained above, each column memory capacitor circuit 45 is constituted by capacitor pair CLS and CLR. There are only as many capacitors as there are columns (y-columns) in the array 15.

Unlike the architecture in a frame-transfer type APS imager, this system requires only as many integrators as there are lines, and hence provides significant advantages over previous systems that required a memory for the entire frame of lines and rows.

In the case of a 1024x1024 imager, only 1024 CLSs (and CLRs) are necessary. Pixel binning is still employed but accomplished without use of an entire stored

frame of pixel values. This is possible, because in full resolution mode, once a row of information makes its way through the CIA block 30 and is sampled in CLS and CLR, the information is immediately read out through the output block by successively turning on CS for successive columns.

CS is essentially a column select signal generated by column select logic 60 that causes the charges stored in CLS and CLR in a selected column to be available to a common global output integrator 70. Global output integrator 70, explained in greater detail below, is a fully differential charge-to-voltage conversion transimpedance amplifier (TIA). Data from each row of the kernel is read out before the next row is sampled on CMS and CMR.

In accordance with a preferred implementation, pixel averaging happens in the row direction first. For instance, assuming a 3x4 kernel selected size, values (signal & reset levels) from three different rows (same column) are successively sampled on CMS and CMR, respectively. Every sampling is followed by an integration. After three cycles, capacitors CIS and CIR hold the accumulated result from the three rows of the kernel. In order to accumulate the signal from these three rows, column-integrators are reset only every third cycle -- i.e. RSTC is closed not in every cycle (since that would erase that data from CIS and CIR), but every third cycle, allowing the capacitors to add to the previous signal. The entire process happens in column parallel fashion, generating summation in the row direction. In order to generate the 3x4 kernel, integration in the column direction needs to be carried out. This is done during readout by simultaneously

closing four adjacent CS signals. Each closure of CS causes the accumulated row values from four neighboring columns to be summed together in the global output integrator 70. It should be readily appreciated that associated column integration switches are embedded in the column select logic 60. An alternative method is to progressively close CS switches, and then successively integrate the adjacent column values in COS and COR. The only difference then is that RST0, the reset switch in the output stage, is closed every fourth cycle (for a 3x4 kernel), instead of every cycle, as might typically be expected.

The kernels can be placed anywhere in the array, and are selected through row and column decoders. Hence, the size and direction of kernels is fully user programmable. In a preferred implementation, the rows and columns are selected in sequential order, however this is easily user definable, and any order could be selected. Random access is a matter of which row and column decoders are selected. Programming the size of the summation kernels is essentially determined by switching.

A timing diagram for generating two adjacent 3x2 kernels is shown in Fig. 3.

During pixel readout, column integrators 35 are reset by pulsing RSTC and RSTC1 high. At that point amplifier A offsets are stored on the capacitors CIS and CIR. When V_{cm} is the common-mode voltage, during the reset phase, the amplifier A offsets force the input of the amplifiers to be: $V_{cm} + V_{offs}$, and $V_{cm} + V_{offr}$, respectively, where identifiers r and s refer to the signal and reset side, the two branches of amplifier A. For reference purposes, signal side shall be at the top

and reset side at the bottom (see Fig. 2). During reset, the potentials across the capacitors are: V+ - V_{cm} - V_{offs}, and V+ - V_{cm} - V_{offr}, respectively. In the next phase, RSTC1B is turned high, connecting the capacitors (CIS and CIR) across the amplifier A. Since the amplifier input nodes remain at the previous levels (i.e., V_{cm} + V_{offs}, and V_{cm} + V_{offr}, respectively), voltages at the output of amplifier A become V+, and are independent of V_{offs} and V_{offr}, indicating the outputs are free from offset. Offset elimination is extremely critical, since one or more columns are summed together. In presence of offset that will vary from one column to another, this will result in an unacceptably high fixed pattern noise in the multi-resolution output.

Following the offset correction phase, ROW 1 is selected. The reset and the signal levels from the pixels in that row are sampled by enabling PHIR and PHIS respectively as shown in Fig. 3. ROW 1 is the first row of the kernel, and can be located anywhere in the pixel array. The signals, sampled on CMR and CMS respectively, are VR and VS. The integration is completed by closing the rowbar CB thereby averaging the contents of the two capacitors CMS and CMR. This causes amplifier A outputs to become:

$$V_{os}(1) = V_{os}(0) + \frac{CMS}{CIS} \cdot \frac{V_R - V_S}{2}$$

$$V_{or}(1) = V_{or}(0) - \frac{CMR}{CIR} \cdot \frac{V_R - V_S}{2}$$

where numbers in parenthesis denote values at the end of a cycle. Identifier 0 is reserved for the reset cycle. As a result of this operation, a signal of (V_R - V_S) is added differentially to both sides of the amplifier branches,

causing the voltage on CIS to go up by $0.5*(V_R - V_S)$ and the voltage on CIR to go down by the same amount. As can be seen from the timing diagram, this process is carried out three (3) times to generate summation for pixels from a given column and three successive rows.

Following the row summing, LDC is pulsed low, sampling the row accumulation signals onto CLS and CLR respectively. At this point the column integrators are reset, preparing them for the next cycle of kernel summing. In order to read two kernels, each of 3x2 size, the successive column selects (CS1 through CS4) are pulsed high. RST0 is used to reset the global amplifier (A0+ and A0-). In order to sum 2 columns, RST0 is pulsed high before CS1 and CS2 are pulsed, ensuring one kernel of 3x2 size is ready for readout. Following this, RST0 is pulsed again to prepare for generation of the second kernel sum, which proceeds along the same lines, except that CS3 and CS4 are pulsed successively, instead of CS1 and CS2.

Each column integrator 35 generally described above includes a fully differential switched-capacitor integrator, a pair of column memory capacitors, CLR and CLS, and the MOS switches (MS, MR, CB, MMS, MMR, MC1, MC2, MC3, MC4, MC7 and MC8) needed for the integration operation. The sample and hold capacitors, CMR and CMS, for the pixel reset and signal levels serve as the input capacitors for each column integrator 35. The column memory capacitors, CLS and CLR, are the input capacitors for the global output integrator 70.

The global output integrator 70 uses two matched single-ended two-stage opamps. The illustrative implementation is configured to drive 30 pF and 1 MW load at above 8 Mpixels/sec required for 30 frames/sec readout

of a 512 x 512 element array. Amplifier A is a folded cascade opamp with switched capacitor common mode feedback circuit. Its operation is set for much lower speed due to the column parallel readout. The designed 2 MHZ unit gain frequency and 60 dB DC gain are sufficient for column parallel integrator settling with better than 9-bit accuracy. The amplifier design is optimized, in a conventional manner, to use minimum transistor size and lowest bias current.

For an n x m (n columns and m rows) kernel summation readout, signals from m rows of the sensor pixel are integrated by the column integrators 35 one row at a time. The reset and signal levels of each row are first sampled on the S/H capacitors CMS and CMR as the integrators 35 are reset. They are then differentially integrated on the integrating capacitors CIS and CIR. This process continues until all the rows in a given kernel are summed. The reset level pertains to the output of the pixel (at the input to the COLUMN block) when it is reset (when RSTP is turned on), and the signal level pertains to that the output of the pixel after the signal charges have been dumped in the sense node.

The integrated signals are sampled and accumulated on the column memory capacitors CLS and CLR. After the row summation is completed, every n consecutive columns are integrated after each reset of the global integrator 70. The summed signals from n x m kernels are read out serially from the output of the global integrator 70. The summation kernel size is programmable according to the illumination condition.

By using a square kernel size of n x n, the S/N enhancement is $\sqrt{n}$. At low illumination, S/N enhancement is greater than $\sqrt{n}$ since the circuit read noise dominates in the imager noise.

The column-wise high residual fixed pattern noise (FPN) is mostly caused by the column opamp offset. In the fully differential readout, the offset is first sampled on the feedback capacitors as the integrator is auto-zeroed. To first order, it is compensated at each step of signal integration. Clock feedthrough appears as common mode pulse to the integrator and does not contribute to FPN. Residual FPN is due to the capacitor ratio mismatch on the two sides of the integrator and is given by,

$$V_{os,o} = m(\alpha_R - \alpha_S)V_C = m\Delta\alpha V_C \quad (1)$$

where m is the number of row summation, Da is the mismatch in capacitor ratio and Vc is the common mode voltage. The temporal read noise consists of noise from the pixel, the detector shot noise, noise associated with switching (kTC noise) and noise from the opamps. The output referred noise for n x m kernel summation can be approximated by,

$$\left\langle V_o^2 \right\rangle \approx n\frac{2kT}{C_M}\alpha^2\left\{2m\alpha^2 + \alpha + 3\beta + 2m(1+\alpha)\beta + mg^2\overline{N}\right\} \quad (2)$$

$C_{MR} = C_{MS} = C_M$; $C_{IR} = C_{IS} = C_I$; $C_{LR} = C_{LS} = C_L$; $C_{OR} = C_{OS} = C_O$; $\alpha = \frac{C_M}{C_I} = \frac{C_L}{C_O}$;

where $\beta = \frac{C_M}{C_L}$; $\overline{N}$ g is the conversion gain measured in volts/electrons; and is the average number of electrons per pixel during a single exposure. The noise

voltage at full resolution readout is estimated to be about 320 MV for 125 frames/sec image readout rate, which is very close to the measured value.

Column-wise fixed pattern noise is caused by the mismatch between the two branches of the amplifier, caused by threshold voltage mismatches. This causes the two differential outputs to be unbalanced around the common-mode level (the ideal average of the output signals). This is corrected by sampling the unbalance in CIS and CIR during reset (RSTC is high).

In another preferred embodiment, a 128 x 128 prototype sensor was implemented by using a 1.2 μm single poly, double metal, n-well process with linear capacitor option. The sensor pixel size was 24 μm x 24 μm with an optical fill factor of 29%. The column circuit was laid out in the 24 mm column pitch and had a total length of about 0.9 mm. The total chip area was about 4.7 mm x 5.2 mm.

The fabricated parts were tested up to 125 frames/sec. The tested readout speed was limited by the capability of the pulse generator and the data acquisition board used in the test bed. The characterization results are summarized in the following table.

Table 1 - Summary of the test results.

Imager format	128 x 128
Integrator linearity:	better than 8 bit out of 1.8 V swing
Sensor saturation:	1.2 V
Temporal Noise:	303 μV r.m.s.
Dynamic range:	72 dB (disregarding FPN)
Conversion gain:	8.3μV/e
Power consumption:	24 mW @ 125 frames/sec
FPN:	6 mV
Dark current:	54 mV/sec (0.6 nA/cm^2

The sensor demonstrates 1.2 V saturation signal, 72 dB dynamic range and 8.3 mV/e- conversion gain. The FPN is about 6 mV (0.5% saturation), read noise 300 MV and dark current 0.6 nA/cm^2. More than 40% of the total 24 mW power is consumed by the global integrator 70 opamps due to the required driving capability.

Figure 4 shows the detailed measurement for signal (mV) and SNR(dB) enhancement as the kernel size is increased from 1 x 1 to 2 x 8 at constant illumination and exposure time. The output signal linearity over 1.2 V range indicates good accuracy of the row and column summation. An 11-dB SNR improvement is achieved, as expected by the theoretical prediction from Equation 2.

In sum, a multi-resolution APS for light adaptive imaging applications has been demonstrated by successfully integrating fully differential opamp based

integrator circuits. Good uniformity and low readout noise was achieved. Enhancement of SNR at low light level was demonstrated to have been achieved by programmable multi-resolution readout at constant frame rate.

The fully differential implementation presented above suppresses clock feedthrough and all other sources of common mode noise, particularly substrate coupling and capacitive coupling noise. Substrate coupling noise arises from variations on power, ground and signal lines, and its magnitude can be significant due to reduction in substrate resistance in nearly all advanced sub-micron CMOS process technologies. In the differential topology presented, the effects of these noise phenomena are suppressed by ensuring that only the difference signal can pass through the circuit. For instance, when signal is sampled on CMS and CMR, charge feedthrough from the switches MS and MR are bound to happen. However, since the switch and capacitance sizes are the same, the feedthrough voltage (Vf) will be nearly the same in both capacitors, especially for small signals where the signals sampled are close to each other. Because the circuit amplifies the difference signal, the common-mode feedthrough (Vf)) does not affect the circuit operation.

In accordance with the presently disclosed implementation, low-noise is achieved by using fully differential circuits so that all extraneous and pick-up noise is eliminated. Low-noise is critical for light-adaptive imaging, since without low noise, pixel binning will not produce sqrt(N) improvement in SNR for low-light level imaging. It should be appreciated that SNR enhancement for an n x n pixel is not sqrt(n) but n, since n^2 pixels are involved.

The imager disclosed herein has extended low-light detection capability, achieved by trading spatial resolution for increased SNR. Unlike the prior art multiresolution chip which produces averaged output and is therefore not suitable for low-light-level signal detection, imager 10 is well adapted for low-light-level signal detection. In the prior art imager, 6 dB attenuation to the signal was calculated which significantly impairs low-light-level signal detection. Imager 10 does not suffer from such attenuation.

When compared to the prior art frame-transfer APS imager with pixel-binning, the current implementation requires no frame buffer memory, thereby reducing the chip size by as much as three fold or more, while preserving pixel-binning capability and reducing read noise. The reduction in area enables large format light adaptive imager implementation without chip size posing limitations, as in previous imager architectures.

In addition, unlike CCD or off-chip summation solutions, the current approach provides orders of magnitude lower power due to use of CMOS imaging technology and low-power analog signal processing circuits. Particularly when compared to known off-chip summation approaches, the preferred implementation provides high speed low-light level data due to reduction of data volume through pixel binning.

Although only a few embodiments have been described in detail below, those having ordinary skill in the art would certainly understand that many modifications are possible in the preferred embodiment without departing from the teachings thereof.

All such modifications are intended to be encompassed by the following claims.

What is claimed is:

1. An active pixel sensor (APS) imager comprising:

a semiconductor substrate;

a pixel sensor array of (x) rows and (y) columns of pixels, formed on said substrate;

a neighborhood selector, formed on said substrate, selecting a kernel of n by m pixels in said array;

a column integrator array, formed on said substrate, defined by a plurality of column integrators, said column integrators coupled to corresponding columns of pixels and operating to differentially integrate pixel signals on each selected row for each pixel block;

a column memory array, formed on said substrate, defined by an array of differentially integrated capacitor circuits, said capacitor circuits summing the differentially integrated pixel signals from the column integrators to generate, at the end of a row summing cycle, a row summed charge signal indicative of said n pixels in said row; and

a global output integrator, formed on said substrate, receiving said row summed charge signal for each of said m columns, and generating a pixel block summed output by summing said (m) signals.

2. The imager of claim 1, wherein said pixel sensor array includes a plurality of pixels, each of which include a photosensor element, and a buffer.

3. The APS imager of claim 1, wherein said neighborhood selector is variable, enabling multiple resolutions of mode imager.

4. The APS imager of claim 1, wherein each column integrator is a differential circuit including a pair of integrating capacitors configured to substantially eliminate extraneous and pick-up noise.

5. The APS imager of claim 4, wherein each capacitor circuit is a fully differential circuit including a pair of summing capacitors.

6. The APS imager of claim 4, wherein each global output integrator is a fully differential circuit including a pair of opamps.

7. The APS imager of claim 1, wherein each pixel block is a square block.

8. The APS imager of claim 1, further comprising column select logic and row select logic generating addressing and timing control signals on the basis of a presently selected resolution mode.

9. The APS imager of claim 1, further comprising column select logic and row select logic generating addressing and timing control signals on the basis of a presently selected pixel block size.

10. A method of operating a pixel sensor, comprising:

obtaining a pixel sensor imager including a pixel sensor array of (x) rows and (y) columns of pixels;

defining a sub block of pixels, of (n) rows and (m) columns of neighboring row and column pixels, where n is less than x and m is less than y;

differentially integrating pixel signals on each of said n rows, using a column integrator array defined by an array of column integrators, said column integrators coupled to said columns of pixels;

summing, said n rows, using a differential integrator, to generate end of a row summing cycle, an (n) row summed charge signal; and

generating a summed output, using a global output integrator, by summing (m) of the n-row charge signals at the end of a column summing cycle.

11. The method of claim 10, further comprising generating addressing and timing control signals on the basis of a presently selected resolution mode.

12. The APS imager of claim 10, further comprising column select logic and row select logic generating addressing and timing control signals on the basis of a presently selected pixel block size.

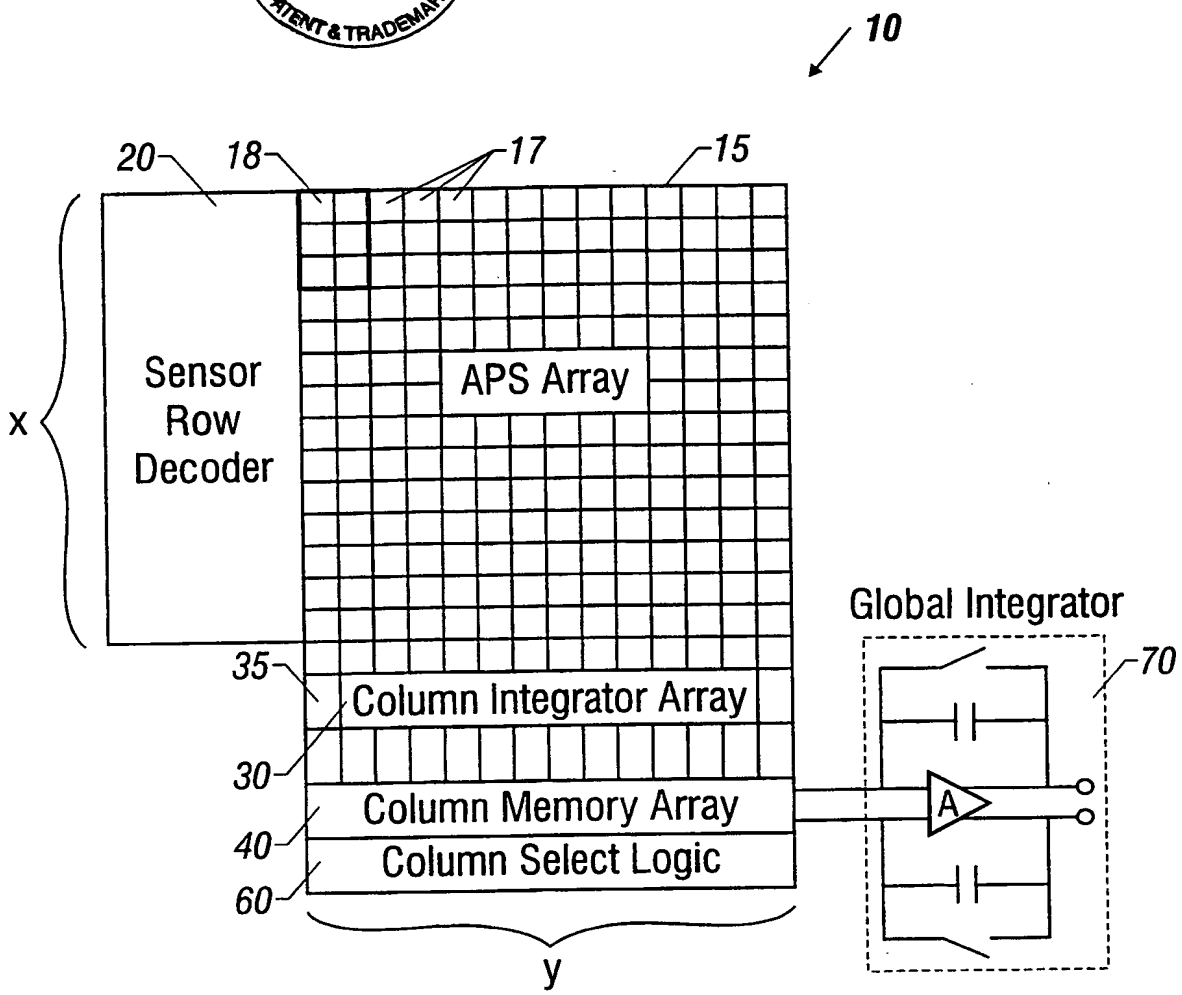


FIG. 1

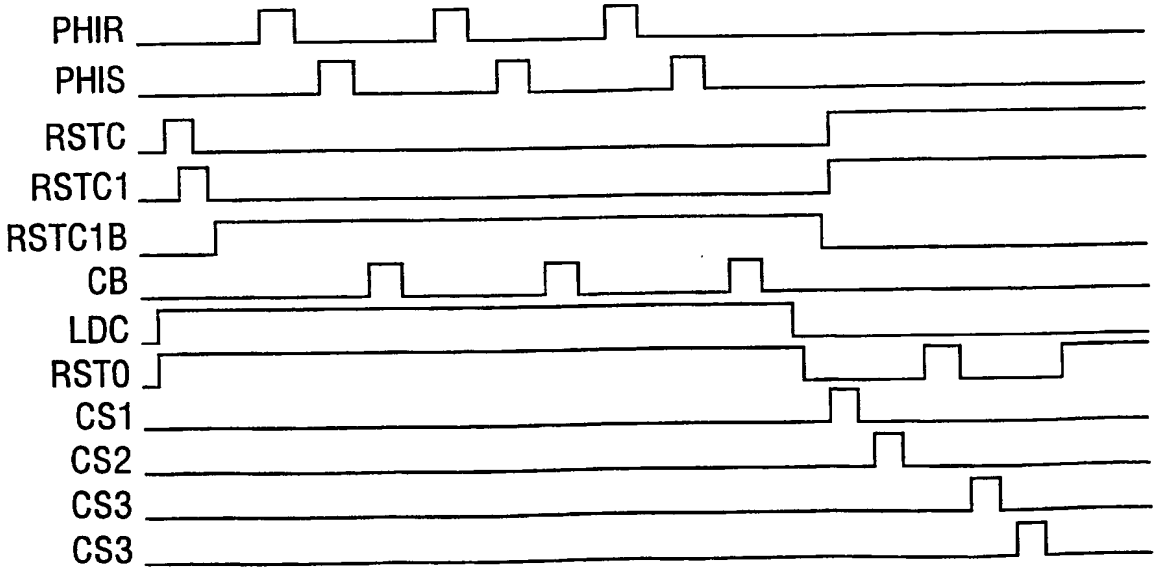
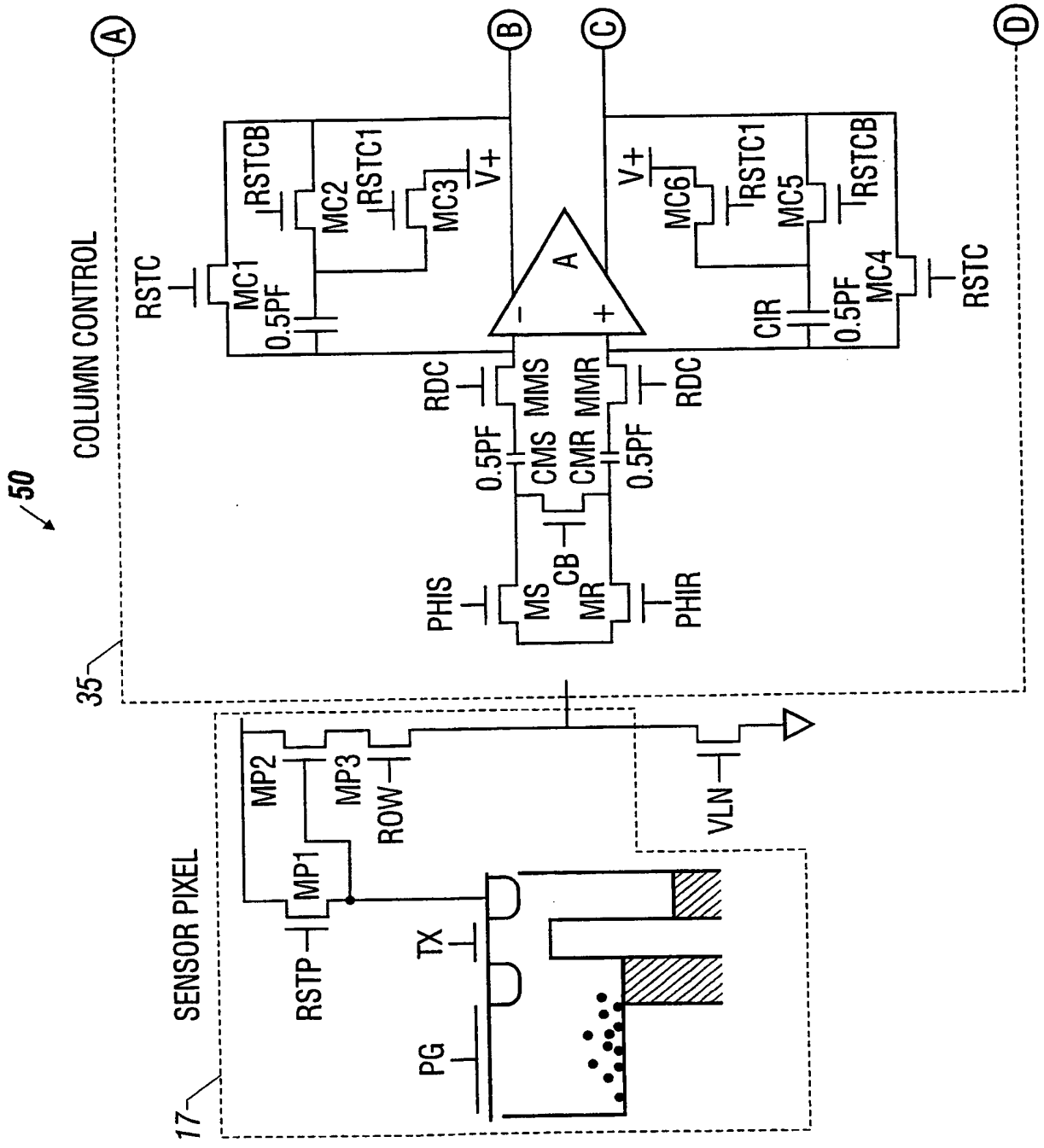


FIG. 3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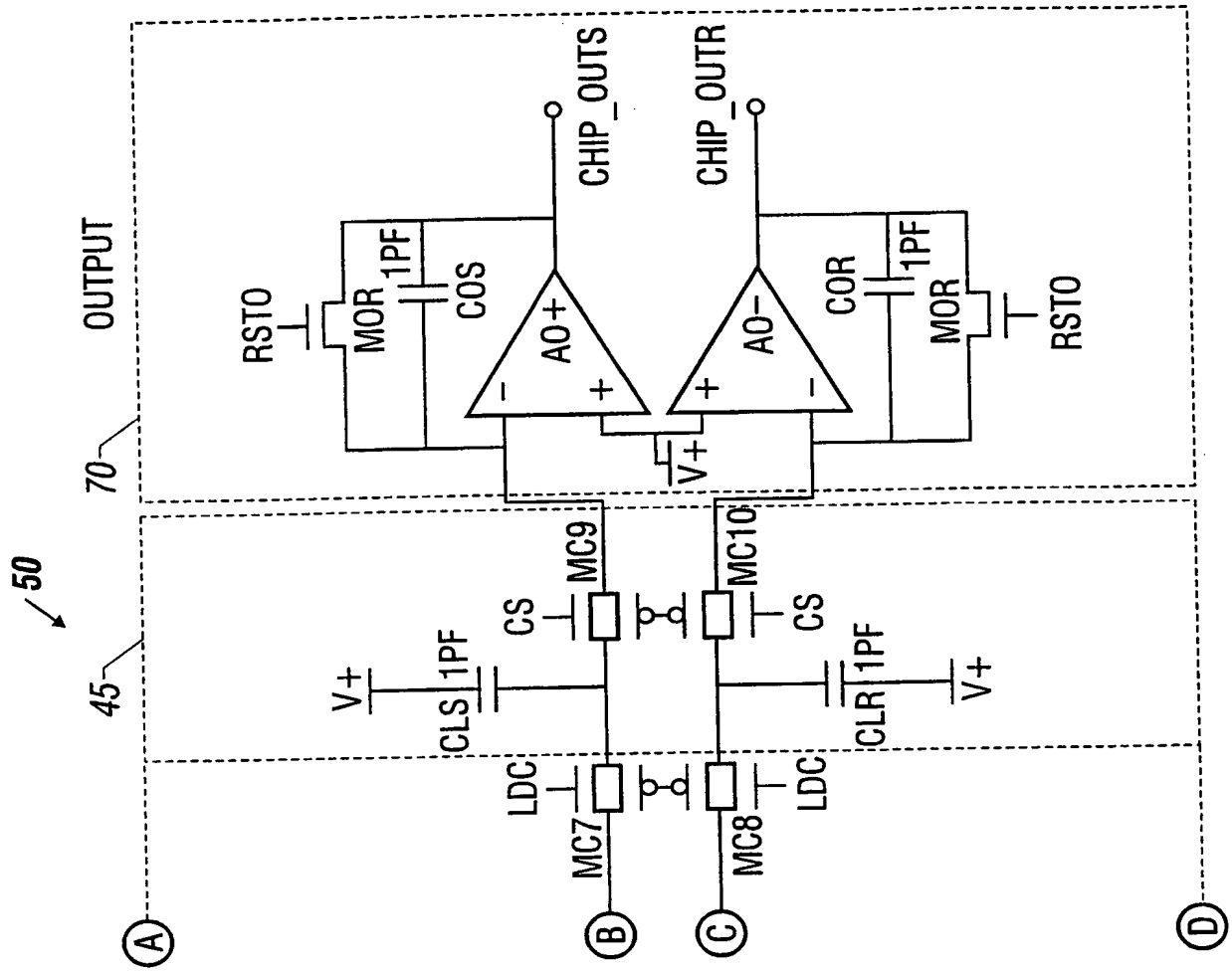
+
V+
MC6
RSTC1
MC5
RSTCB
CIR
0.5PF
MC4
RSTC
RDC
0.5PF
MMS
CMS
CMR
MMR
0.5PF
RDC
PHIS
MS
CB
MR
PHIR
35
MP2
MP3
ROW
VLN
SENSOR PIXEL
MP1
RSTP
TX
PG
17

FIG. 2A

FIG. 2B


50
OUTPUT
70
45
CHIP_OUTS
CHIP_OUTR
RSTO
MOR
1PF
COS
AO+
AO-
COR
V+
MC9
MC10
CS
CLS
CLR
LDC
MC7
MC8
A
B
C
D

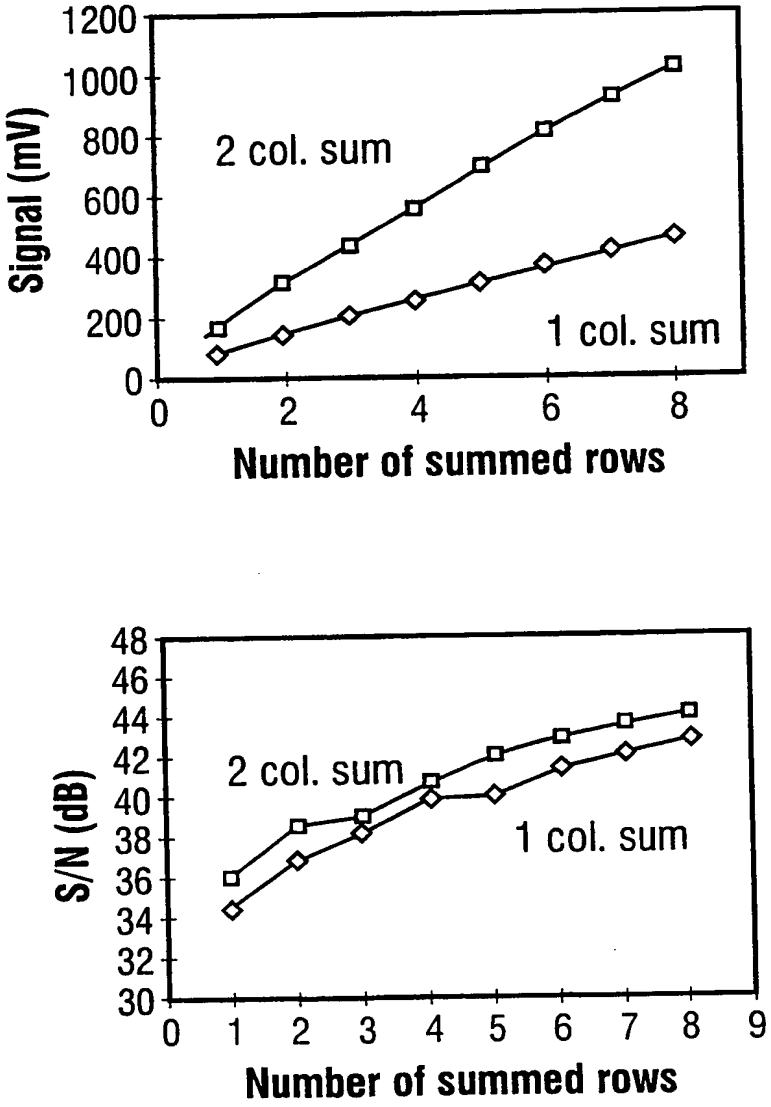

1200
1000
800
600
400
200
0
Signal (mV)
2 col. sum
1 col. sum
0
2
4
6
8
Number of summed rows
48
46
44
42
40
38
36
34
32
30
S/N (dB)
2 col. sum
1 col. sum
0
1
2
3
4
5
6
7
8
9
Number of summed rows

FIG. 4

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US99/05830

A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) :H04N 3/14
US CL : 348/294, 295, 297, 300, 302, 307, 308

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 348/294, 295, 297, 300, 302, 307, 308

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 5,471,515 A (FOSSUM et al.) 28 November 1995	1-12
A	US 5,402,171 A (TAGAMI et al.) 28 March 1995	1-12
A, E	US 5,920,345 A (SAUER) 06 July 1999	1-12
A, E	US 5,917,547 A (MERRILL et al.) 29 June 1999	1-12
A, E	US 5,900,623 A (TSANG et al.) 04 May 1999	1-12
A, E	US 5,896,173 A (HASSLER) 20 April 1999	1-12
A, E	US 5,892,540 A (KOZLOWSKI et al.) 06 April 1999	1-12
A, E	US 5,883,668 A (KAZAMA et al.) 16 March 1999	1-12

[X] Further documents are listed in the continuation of Box C. [ ] See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E"	earlier document published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search 16 JULY 1999	Date of mailing of the international search report 17 AUG 1999
Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. (703) 305-3230	Authorized officer JACQUELINE WILSON Telephone No. (703) 308-5080

Form PCT/ISA/210 (second sheet)(July 1992)*

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US99/05830

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A, E	US 5,877,715 A (GOWDA et al.) 02 March 1999	1-12
A, P	US 5,841,126 A (FOSSUM et al.) 24 November 1998	1-12
A	US 5,434,620 A (HIGUCHI et al.) 18 July 1995	1-12
A, E	US 5,909,026 A (ZHOU et al.) 01 June 1999	1-12

From the INTERNATIONAL BUREAU

NOTIFICATION CONCERNING TRANSMITTAL OF COPY OF INTERNATIONAL PRELIMINARY REPORT ON PATENTABILITY (CHAPTER I OF THE PATENT COOPERATION TREATY)
(PCT Rule 44bis.1(c))

To:

D'AMICO, Thomas, J.
Dickstein Shapiro Morin & Oshinsky LLP
2101 L Street, NW
Washington, DC 20037-1526
ETATS-UNIS D'AMERIQUE

Date of mailing *(day/month/year)*	
26 May 2006 (26.05.2006)	
Applicant's or agent's file reference	IMPORTANT NOTICE
M4 0650960P960PC	

International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/US2004/037729	12 November 2004 (12.11.2004)	13 November 2003 (13.11.2003)

Applicant
MICRON TECHNOLOGY, INC. et al

The International Bureau transmits herewith a copy of the international preliminary report on patentability (Chapter I of the Patent Cooperation Treaty)

The International Bureau of WIPO
34, chemin des Colombettes
1211 Geneva 20, Switzerland

Facsimile No. +41 22 740 14 35

Authorized officer
Yolaine Cussac

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PATENT COOPERATION TREATY

PCT

INTERNATIONAL PRELIMINARY REPORT ON PATENTABILITY

(Chapter I of the Patent Cooperation Treaty)

(PCT Rule 44*bis*)

Applicant's or agent's file reference M4 0650960P960PC	**FOR FURTHER ACTION**	See item 4 below
International application No. PCT/US2004/037729	International filing date *(day/month/year)* 12 November 2004 (12.11.2004)	Priority date *(day/month/year)* 13 November 2003 (13.11.2003)
International Patent Classification (8th edition unless older edition indicated) See relevant information in Form PCT/ISA/237		
Applicant MICRON TECHNOLOGY, INC.		

1. This international preliminary report on patentability (Chapter I) is issued by the International Bureau on behalf of the International Searching Authority under Rule 44 *bis*.1(a).

2. This REPORT consists of a total of 6 sheets, including this cover sheet.

   In the attached sheets, any reference to the written opinion of the International Searching Authority should be read as a reference to the international preliminary report on patentability (Chapter I) instead.

3. This report contains indications relating to the following items:

☒	Box No. I	Basis of the report
☐	Box No. II	Priority
☐	Box No. III	Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
☐	Box No. IV	Lack of unity of invention
☒	Box No. V	Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
☐	Box No. VI	Certain documents cited
☐	Box No. VII	Certain defects in the international application
☐	Box No. VIII	Certain observations on the international application

4. The International Bureau will communicate this report to designated Offices in accordance with Rules 44*bis*.3(c) and 93*bis*.1 but not, except where the applicant makes an express request under Article 23(2), before the expiration of 30 months from the priority date (Rule 44*bis* .2).

	Date of issuance of this report 15 May 2006 (15.05.2006)
The International Bureau of WIPO 34, chemin des Colombettes 1211 Geneva 20, Switzerland Facsimile No. +41 22 740 14 35	Authorized officer Yolaine Cussac Telephone No. +41 22 338 70 80

Form PCT/IB/373 (January 2004)

PATENT COOPERATION TREATY

REC'D 02 FEB 2005

WIPO PCT

From the
INTERNATIONAL SEARCHING AUTHORITY

13/05

PCT

To:

see form PCT/ISA/220

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

(PCT Rule 43*bis*.1)

	Date of mailing *(day/month/year)* see form PCT/ISA/210 (second sheet)
Applicant's or agent's file reference see form PCT/ISA/220	**FOR FURTHER ACTION** See paragraph 2 below

International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/US2004/037729	12.11.2004	13.11.2003

International Patent Classification (IPC) or both national classification and IPC
H04N3/15

Applicant
MICRON TECHNOLOGY, INC.

1. This opinion contains indications relating to the following items:

- ☒ Box No. I Basis of the opinion
- ☐ Box No. II Priority
- ☐ Box No. III Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
- ☐ Box No. IV Lack of unity of invention
- ☒ Box No. V Reasoned statement under Rule 43*bis*.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
- ☐ Box No. VI Certain documents cited
- ☐ Box No. VII Certain defects in the international application
- ☐ Box No. VIII Certain observations on the international application

2. **FURTHER ACTION**

If a demand for international preliminary examination is made, this opinion will usually be considered to be a written opinion of the International Preliminary Examining Authority ("IPEA"). However, this does not apply where the applicant chooses an Authority other than this one to be the IPEA and the chosen IPEA has notifed the International Bureau under Rule 66.1*bis*(b) that written opinions of this International Searching Authority will not be so considered.

If this opinion is, as provided above, considered to be a written opinion of the IPEA, the applicant is invited to submit to the IPEA a written reply together, where appropriate, with amendments, before the expiration of three months from the date of mailing of Form PCT/ISA/220 or before the expiration of 22 months from the priority date, whichever expires later.

For further options, see Form PCT/ISA/220.

3. For further details, see notes to Form PCT/ISA/220.

Name and mailing address of the ISA:

European Patent Office - P.B. 5818 Patentlaan 2
NL-2280 HV Rijswijk - Pays Bas
Tel. +31 70 340 - 2040 Tx: 31 651 epo nl
Fax: +31 70 340 - 3016

Authorized Officer

Bequet, T

Telephone No. +31 70 340-3339

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US2004/037729

Box No. I Basis of the opinion

1. With regard to the **language**, this opinion has been established on the basis of the international application in the language in which it was filed, unless otherwise indicated under this item.

   ☐ This opinion has been established on the basis of a translation from the original language into the following language , which is the language of a translation furnished for the purposes of international search (under Rules 12.3 and 23.1(b)).

2. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application and necessary to the claimed invention, this opinion has been established on the basis of:

   a. type of material:

   ☐ a sequence listing

   ☐ table(s) related to the sequence listing

   b. format of material:

   ☐ in written format

   ☐ in computer readable form

   c. time of filing/furnishing:

   ☐ contained in the international application as filed.

   ☐ filed together with the international application in computer readable form.

   ☐ furnished subsequently to this Authority for the purposes of search.

3. ☐ In addition, in the case that more than one version or copy of a sequence listing and/or table relating thereto has been filed or furnished, the required statements that the information in the subsequent or additional copies is identical to that in the application as filed or does not go beyond the application as filed, as appropriate, were furnished.

4. Additional comments:

Box No. V Reasoned statement under Rule 43*bis*.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Yes:	Claims	7-9,13-19,23-25,28-30,34-36
	No:	Claims	1-6,10-12,20-22,26,27,31-33
Inventive step (IS)	Yes:	Claims	
	No:	Claims	7-9,13-19,23-25,28-30,34-36
Industrial applicability (IA)	Yes:	Claims	1-36
	No:	Claims	

2. Citations and explanations

see separate sheet

Re Item V.

1) The following documents are referred to in this communication:
D1 : US 6 377 304 B1 (SAITOH AKIHIRO) 23 April 2002 (2002-04-23)
D2 : WO 99/48281 A1 (CALIFORNIA INSTITUTE OF TECHNOLOGY) 23 September 1999 (1999-09-23)
D3 : US 5 949 483 A (FOSSUM ET AL) 7 September 1999

2) Although claims 1, 6, 10, 20, 26, 31 have been drafted as separate independent claims, they appear to relate effectively to the same subject-matter and to differ from each other only with regard to the definition of the subject-matter for which protection is sought ..and/or.. in respect of the terminology used for the features of that subject-matter. The aforementioned claims therefore lack conciseness and as such do not meet the requirements of Article 6 PCT.

3) The present application does not meet the criteria of Article 33(1) PCT, because the subject-matter of independant claims 1, 10, 20, 26, 31 is not new in the sense of Article 33(2) PCT.

3.1) In the technical field of image sensors two different possibilities exist for reducing the bandwidth or increasing the frame rate : sub-sampling and binning. The present application relates to the second alternative.

3.2) D1 which is considered as the closest prior art (it has been chosen because the S/H circuits contain a plurality of capacitors for each type of signal) discloses an image sensor readout circuit comprising:

a column line (fig.7, 15) for receiving a plurality of analog signals (image and reset signals of an APS),

a binning circuit (32, 35, H1, H2, col.14, lines 46-52, col.14, line 64-col.15, line 10)) coupled to said column, combining pixel signals from capacitors (34s, 35s, H1, H2) and outputting them on a first output line (38s) and combining the reset signals from capacitors (34d, 35d, H1, H2) and outputting them on a second output line 38(d).

All the features of claim 1 being known from D1 it is therefore not new.

The same objection is valid for the remaining independant claims (10, 20, 26, 31), which are considered as equivalent.

It should be noted that these claims are also anticipated by D2 and D3, which means that averaging the pixel signals **and** the corresponding reset signals when performing a binning is well known.

3.3) Relating to claim 6 D3 appears to be the closest prior art, it discloses two sample circuits for storing a plurality of pixel/reset signals, once the data corresponding to a plurality of rows have been integrated, they are connected to bus lines 720, 720' which are themselves connected to a differential amplifier 726 (col.13, lines 38-54), all the features of claim 6 being known from D3 it is therefore not new.

4) In the remaining dependant claims structural details to the apparatus defined in the independant claims are set out, all of which insofar as they are not explicitly disclosed in D1-D3 relate to routine measures normally to be expected from the skilled person. Thus these claim lack novelty or inventive step.

4.1) More particularly referring to claims 2-5, D1 (fig.7) also discloses a plurality of capacitors connected to the same plurality of sampling switches said plurality of capacitors/switches being an even number.

Claims 7-9 are known from D1, these claims are therefore not inventive.

Claims 11-12 are known from D1,

the colour aspect defined in claims 13-19 is considered as not inventive because when performing a binning the skilled person is aware that only identical colour values can be averaged for keeping the colour integrity,

claims 21, 22, 27, 32, 33 are also explicitly disclosed in D1.